



Features

- Hot pluggable CFP4 MSA form factor
- Compliant to IEEE 802.3bm 100GBASE-SR4
- Supports 103.1Gb/s aggregate bit rate
- Up to 100m OM4 MMF transmission
- Single +3.3V power supply
- Operating case temperature: 0 to 70°C
- 4x25G electrical interface (CEI-28G-VSR)
- MDIO management interface with digital diagnostic monitoring
- Maximum power consumption 3.5W
- MTP/MPO optical connector
- RoHS-6 compliant

Applications

- 100GBASE-SR4 Ethernet

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T _s	-40	85	°C	
Relative Humidity (non-condensation)	RH	0	85	%	
Operating Case Temperature	T _{op}	0	70	°C	
Supply Voltage	V _{cc}	-0.5	3.6	V	
Voltage on LVTTTL Input	V _{ilvttl}	-0.5	VCC3+0.3	V	
LVTTTL Output Current	I _{olvttl}		15	mA	
Voltage on Open Collector Output	V _{oco}	0	6	V	
Damage Threshold, each Lane	TH _d	3.4		dBm	1

Notes:

1. PIN receiver.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Operating Case Temperature	T _{op}	0		70	°C	
Power Supply Voltage	V _{cc}	3.135	3.3	3.465	V	
Data Rate, each Lane			25.78125		Gb/s	
Data Rate Accuracy		-100		100	ppm	
Control Input Voltage High		2		V _{cc}	V	
Control Input Voltage Low		0		0.8	V	
Power Supply Noise	V _{rip}			2	%	DC-1MHz
				3	%	1-10MHz
Link Distance (OM3 MMF)	D1			70	m	
Link Distance (OM4 MMF)	D2			100	m	

Diagnostics Monitoring

Parameter	Symbol	Accuracy	Unit	Notes
Temperature monitor absolute error	DMI_Temp	± 3	°C	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	± 0.15	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	± 2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	± 10%	mA	Ch1~Ch4
Channel TX power monitor absolute error	DMI_TX_Ch	± 2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Transmitter Electro-Optical Characteristics (each Lane)

Parameter	Test Point	Min	Typ.	Max	Units	Notes
Power Consumption				3.5	W	
Supply Current	I _{cc}			1.06	A	
Low Power Mode Power Dissipation				1.0	W	
Overload Differential Voltage pk-pk	TP1a	900			mV	
Common Mode Voltage (V _{cm})	TP1	-350		2850	mV	1
Differential Termination Resistance Mismatch	TP1			10	%	At 1MHz
Differential Return Loss (SDD11)	TP1			See CEI-28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)	TP1			See CEI-28G-VSR Equation 13-20	dB	
Stressed Input Test	TP1a		See CEI-28G-VSR Section 13.3.11.2.1			
Center Wavelength	λ_c	840	850	860	nm	
RMS Spectral Width	$\Delta\lambda_{rms}$			0.6	nm	
Average Launch Power, each Lane	P _{AVG}	-8.4		2.4	dBm	
Optical Modulation Amplitude (OMA), each Lane	P _{OMA}	-6.4		3.0	dBm	2
Launch Power in OMA minus TDEC, each Lane		-7.3			dBm	
Transmitter and Dispersion Eye Closure (TDEC), each Lane				4.3	dB	
Extinction Ratio	ER	2.0			dB	
Optical Return Loss Tolerance	TOL			12	dB	
Average Launch Power OFF Transmitter, each Lane	P _{off}			-30	dBm	
Encircled Flux				$\geq 86\%$ at 19 μ m $\leq 30\%$ at 4.5 μ m		

<i>Parameter</i>	<i>Test Point</i>	<i>Min</i>	<i>Typ.</i>	<i>Max</i>	<i>Units</i>	<i>Notes</i>
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}				3

Notes:

1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. Even if the TDP < 0.9 dB, the OMA min must exceed the minimum value specified here.
3. Hit ratio 1.5×10^{-3} hits per sample.

Receiver Electro-Optical Characteristics (each Lane)

Parameter	Test Point	Min	Typ.	Max	Units	Notes
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (Vcm)	TP4	-350		2850	mV	1
Common Mode Noise, RMS	TP4			17.5	mV	
Differential Termination Resistance Mismatch	TP4			10	%	At 1MHz
Differential Return Loss (SDD22)	TP4			See CEI-28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)	TP4			See CEI-28G-VSR Equation 13-21	dB	
Common Mode Return Loss (SCC22)	TP4			-2	dB	2
Transition Time, 20 to 80%	TP4	9.5			ps	
Vertical Eye Closure (VEC)	TP4			5.5	dB	
Eye Width at 10 ⁻¹⁵ probability (EW15)	TP4	0.57			UI	
Eye Height at 10 ⁻¹⁵ probability (EH15)	TP4	228			mV	
Center Wavelength	λ_c	840	850	860	nm	
Damage Threshold, each Lane	TH _d	3.4			dBm	3
Average Receive Power, each Lane		-10.3		2.4	dBm	
Receive Power (OMA), each Lane				3.0	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-9.2	dBm	For BER=5x10 ⁻⁵
Stressed Receiver Sensitivity (OMA), each Lane				-5.2	dBm	4
Receiver Reflectance	R _R			-12	dB	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	

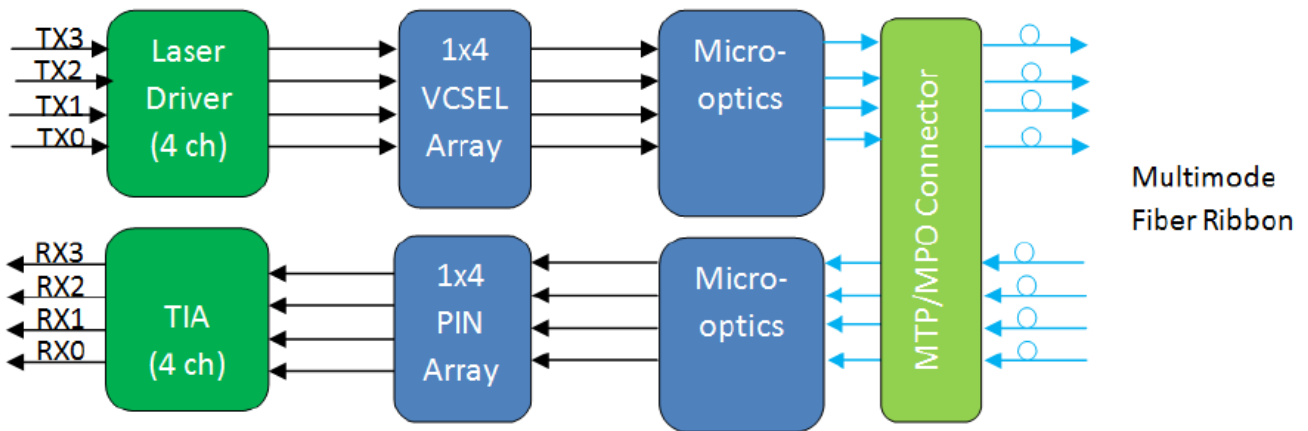
Conditions of Stress Receiver Sensitivity Test (Note 5)

Stressed Eye Closure (SEC), Lane under Test	4.3	dB
Stressed Eye J2 Jitter, Lane under Test	0.39	UI
Stressed Eye J4 Jitter, Lane under Test	0.53	UI
OMA of each Aggressor Lane	3	dBm
Stressed Receiver Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}, Hit ratio 5×10^{-5} hits per sample	{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}	

Notes:

1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. From 250MHz to 30GHz.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = 5×10^{-5}
5. Vertical eye closure penalty, stressed eye J2 jitter, stressed eye J4 jitter, and stressed receiver eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Block Diagram of Transceiver



This product is a 100Gb/s transceiver module for optical communication applications compliant to 100GBASE-SR4 of the IEEE P802.3bm standard. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of VCSEL optical signals over 4 multimode fibers for 100Gb/s optical transmission. Reversely, on the receiver side, the module receives 4 channels of VCSEL optical signals over 4 multimode fibers and then converts them to 4 output channels of 25Gb/s electrical data.

The high speed VCSEL transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 100m links over OM4 multimode fibers and compliant to optical interface with IEEE802.3bm Clause 95 100GBASE-SR4 requirements.

The product is designed with form factor, optical/electrical connection and MDIO interface according to the CFP4 Multi-Source Agreement (MSA). The innovative design has all the fibers inside the CFP4 package configured without any splicing or non-permanent connector. Also, fiber routines are neatly organized and fixed inside a stainless steel container.

This product contains an MTP/MPO optical connector for the optical interface and a 56-pin connector for the electrical interface. Figure 1 in Section 3 shows the functional block diagram of this product.

Transmitter Operation

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock and Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently, each of 4 EML laser driver IC's converts one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 VCSEL lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches an optical signal whose characteristics are compliant to IEEE802.3bm 100GBASE-SR4 requirements. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or through MDIO module management interface.

Receiver Operation

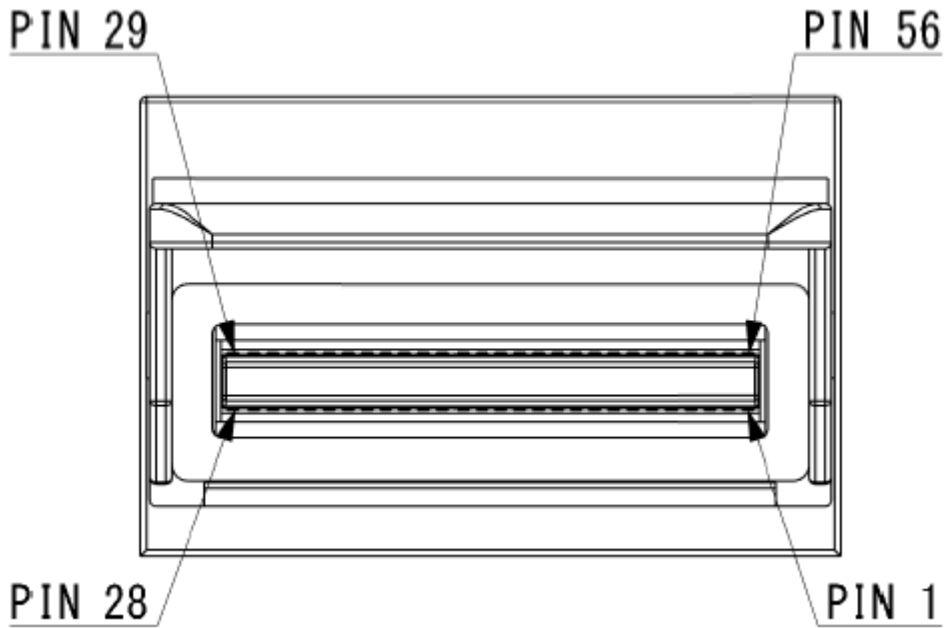
The receiver receives 4 channels of VCSEL optical signals over 4 multimode fibers and each of the 4 channels of optical signals is fed into one of the 4 receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by the RX portion of the 4-channel CDR. The retimed 4-lane output electrical signals are compliant with IEEE CAUI-4 interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value is reported through the MDIO section. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

MDIO Interface Pins

The CFP4 module supports the MDIO interface specified in IEEE802.3bm Clause 45. It supports alarm, control and monitor functions via hardware pins and via an MDIO bus. Upon module initialization, these functions are available. CFP4 MDIO electrical interface consists of 6 wires including 2 wires of MDC and MDIO, as well as 3 Port Address wires, and the Global Alarm wire. MDC is the MDIO Clock line driven by host and MDIO is the bidirectional data line driven by both host and module depending upon the data directions. The CFP4 uses pins in the electrical connector to instantiate the MDIO interface as listed in below table.

PIN	Symbol	Description	I/O	Logic	“H”	“L”
13	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm
18	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS		
17	MDC	MDIO Clock	I	1.2V LVCMOS		
19	PRTADR0	MDIO port address bit 0	I	1.2V LVCMOS	per MDIO document	
20	PRTADR1	MDIO port address bit 1	I	1.2V LVCMOS		
21	PRTADR2	MDIO port address bit 2	I	1.2V LVCMOS		

Pin Orientation



Pin Map

CFP4		CFP4	
Bottom		Top	
1	3.3V_GND	56	GND
2	3.3V_GND	55	TX3n
3	3.3V	54	TX3p
4	3.3V	53	GND
5	3.3V	52	TX2n
6	3.3V	51	TX2p
7	3.3V_GND	50	GND
8	3.3V_GND	49	TX1n
9	VND IO A	48	TX1p
10	VND IO B	47	GND
11	TX DIS (PRG CNTL1)	46	TX0n
12	RX LOS (PRG ALRM1)	45	TX0p
13	GLB ALRMn	44	GND
14	MOD LOPWR	43	(REFCLKn)
15	MOD ABS	42	(REFCLKp)
16	MOD_RSTn	41	GND
17	MDC	40	RX3n
18	MDIO	39	RX3p
19	PRTADR0	38	GND
20	PRTADR1	37	RX2n
21	PRTADR2	36	RX2p
22	VND IO C	35	GND
23	VND IO D	34	RX1n
24	VND IO E	33	RX1p
25	GND	32	GND
26	(MCLKn)	31	RX0n
27	(MCLKp)	30	RX0p
28	GND	29	GND

Definition of the Bottom Side Pins from Pin 1 through Pin 28

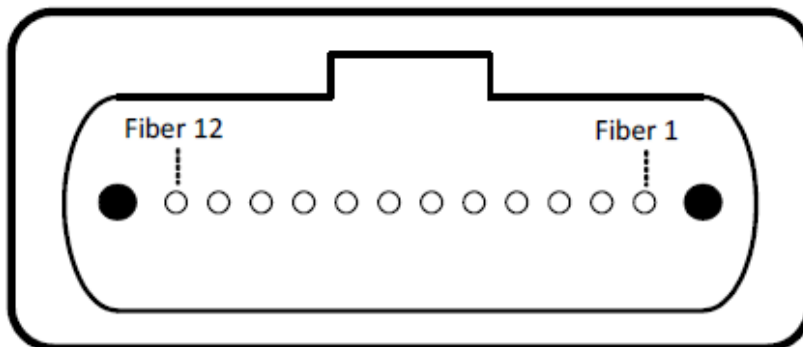
PIN	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
2	3.3V_GND			
3	3.3V			
4	3.3V			
5	3.3V			
6	3.3V			3.3V Module Supply Voltage
7	3.3V_GND			
8	3.3V_GND			
9	VIND_IO_A	I/O		Module Vendor I/O A. Do Not Connect
10	VIND_IO_B	I/O		Module Vendor I/O B. Do Not Connect
11	TX_DIS (PRG_CNTL1)	I	LVC MOS w/PUR	Transmitter Disable for all lanes. "1" or NC: Transmitter disabled; "0": transmitter enabled. (Optionally configurable as Programmable Control1 after Reset)
12	RX_LOS (PRG_ALRM1)	O	LVC MOS w/PUR	Receiver Loss of Optical Signal. "1": low optical signal; "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset)
13	GLB_ALRMn	O	LVC MOS	Global Alarm. "0": alarm condition in any MDIO Alarm register; "1": no alarm condition, Open Drain, Pull up Resistor on Host
14	MOD_LOPWR	I	LVC MOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode; "0": power-on enabled
15	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent; "0": module present, Pull up resistor on Host
16	MOD_RSTn	I	LVC MOS w/PDR	Module Reset. "0": resets the module; "1" or NC: module enabled, Pull down Resistor in Module
17	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
18	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)
19	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
20	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
21	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
22	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
23	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect
24	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect
25	GND			
26	(MCLKn)	O	CML	For optical waveform testing. Not for normal use
27	(MCLKp)	O	CML	For optical waveform testing. Not for normal use
28	GND			

Definition of Top Side Pins

PIN	Name	PIN	Name
29	GND	43	(REFCLKp)
30	RX0p	44	GND
31	RX0n	45	TX0p
32	GND	46	TX0n
33	RX1p	47	GND
34	RX1n	48	TX1p
35	GND	49	TX1n
36	RX2p	50	GND
37	RX2n	51	TX2p
38	GND	52	TX2n
39	RX3p	53	GND
40	RX3n	54	TX3p
41	GND	55	TX3n
42	(REFCLKn)	56	GND

Optical Interface Lanes and Assignment

Figure below shows the orientation of the multi-mode fiber facets of the optical connector. Table below provides the lane assignment.

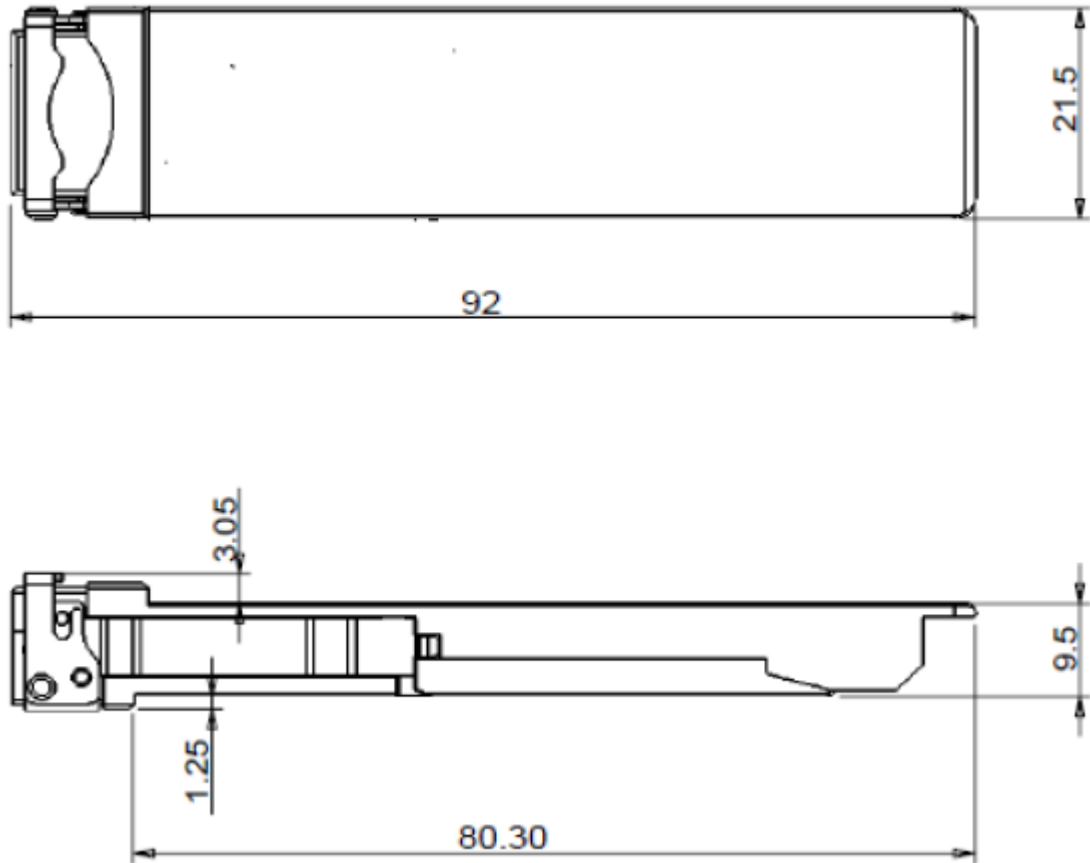


Outside View of the CFP4 Module MPO Receptacle

Table: Lane assignment


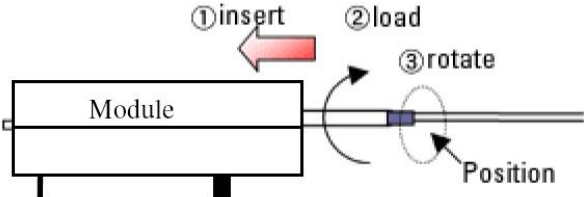
Fiber #	Lane Assignment
1	RX0
2	RX1
3	RX2
4	RX3
5	Not used
6	Not used
7	Not used
8	Not used
9	TX3
10	TX2
11	TX1
12	TX0

Dimensions



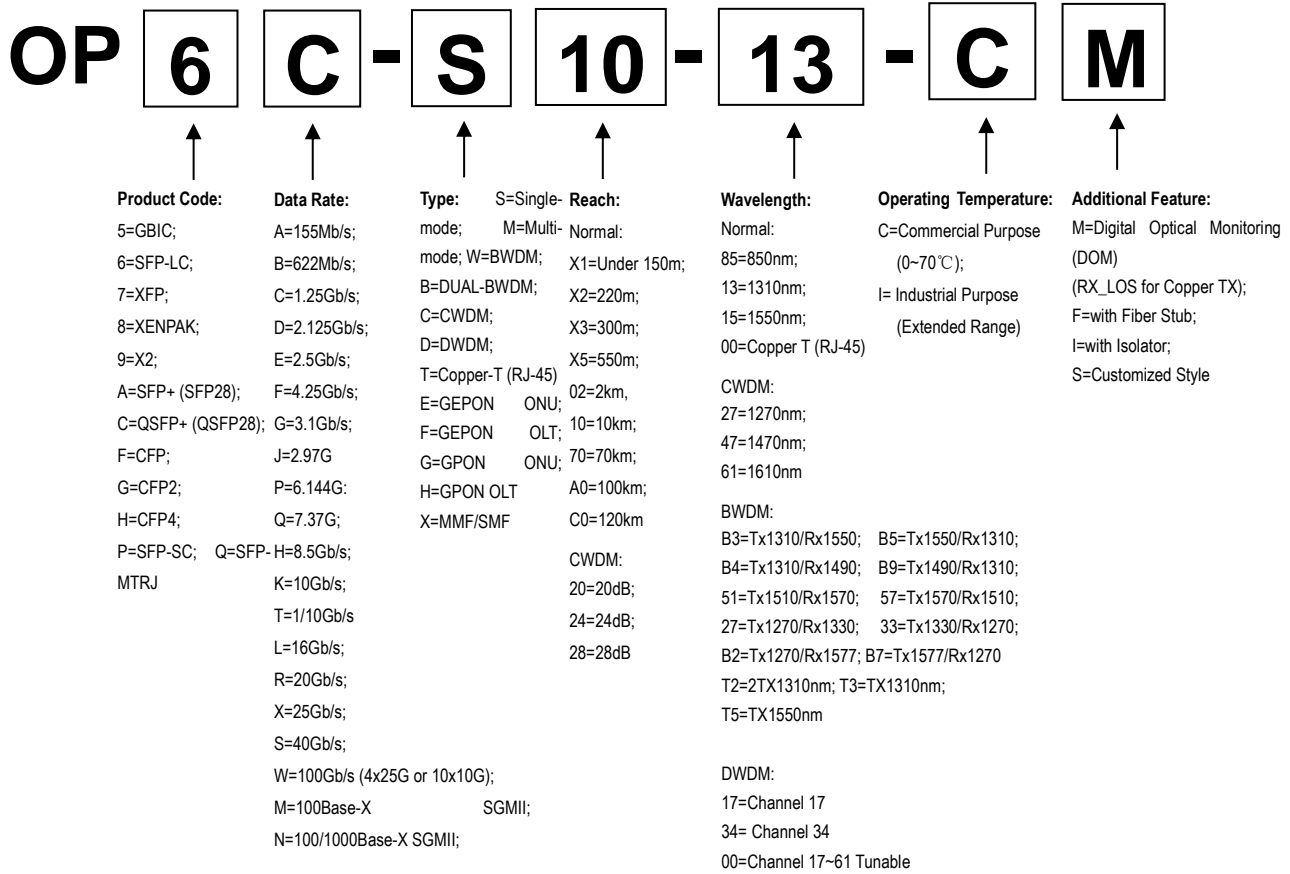
Optical Receptacle Cleaning Recommendations :

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.

<p>Cleaning of patch-cord</p> 	<p>Cleaning of fiber stub</p>  <ol style="list-style-type: none"> 1. Insert Ensure that stick is held straight when inserting into sleeve. 2. Load Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve. 3. Rotate Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained. <p><i>Notice: Number of possible wipes: Maintenance (repair) ~1 use / piece Equipment construction: 4 uses / piece (max.)</i></p>
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Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information



Model Number	Part Number	Voltage	Temperature
CFP4-100G-SR4	OPHW-MX1-85-CB	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.